

**REMARKS/ARGUMENTS**

Request for Continued Examination:

The applicant respectfully requests continued examination of the above-indicated application as per 37 CFR 1.114.

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**1. Claim Rejections – 35 USC 103**

Claims 1, 3, 7, 11-14, 19-21, and 23-24 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over DeKoning et al. (US Patent No. 6,467,023, DeKoning for short hereafter) in view of Randall et al. (US Patent No. 6,530,031, Randall for short hereafter).

Claims 2, 4-6, 18 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over DeKoning in view of Randall as applied to claim 1 above, and further in view of TechTarget (“Nonvolatile Storage”, TechTarget for short hereafter).

Claims 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over DeKoning in view of Randall as applied to claim 7 above, and further in view of TechTarget.

Claims 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over DeKoning in view of Randall as applied to claim 3 above, and further in view of TechTarget.

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over DeKoning in view of Randall in view of TechTarget as applied to claim 2 above, and further in view of Humlicek et al. (US Patent No. 5,822,782).

**Response:**

Claim 1

To speed up the prosecution of the instant application, claim 1 has been amended to specify that “data in the initialization regions of the RAID are made consistent with one another by the consistency initialization”. The applicant respectfully adds the features that are mentioned by the Examiner in the Office Action mailed on August 5, 2010, to amend claim 1 to meet the request of the Examiner (Please refer to page 20, lines 1-6 of the OA, “In response to applicant’s argument that the references fail to show certain features of applicant’s invention, it is noted that the features upon which applicant relies (i.e.,

initialization table that records consistency initialization which means data in the regions of a RAID subsystem are made consistent with one another by the consistency initialization) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the 5 claims". As no new matter is introduced, consideration of the above-identified claim amendments is respectfully requested. In addition, the applicant believes that the amended claim 1 conforms to the Examiner's request, so that the amended claim 1 is believed to be patentably distinct from the cited references and is now in condition for allowance.

10        The applicant respectfully points out that the interpretation of the initialization progress table has already been stated in claim 1 since claim 1 teaches "the initialization progress table including a plurality of fields for storing initialization states of each of a plurality of initialization regions of the RAID so as to indicate which initialization regions have been initialized by a regional initialization and which initialization regions have not 15 yet been initialized"; therefore, the interpretation of the initialization progress table has already been stated in claim 1 that the initialization progress table includes a plurality of fields and is for storing initialization states of each of a plurality of initialization regions of the RAID, and the result is that the initialization progress table is used to indicate which initialization regions have been initialized by a regional initialization and which 20 initialization regions have not yet been initialized.

With regard to teachings of Randall, the applicant respectfully points out that Randall expressly teaches: "The present invention discloses a method and apparatus to provide accurate and automated timing of firmware routines, such as initialization tasks at boot time. Since each task sends a progress indicator code to a display buffer when it 25 starts to run, by saving processor time stamps at the time these codes change, it is possible to calculate and store the time duration for each routine. In the case of system initialization, these time durations can be an indication of problems if they are much longer than normal or an indication of excessive, inefficient, or ineffective processing that might be speeded up in order to reduce the total boot time. [see column 2, lines 30 19-29]", "After loading the first initialization program from ROM (step 300), each

initialization task calls a routine to display a progress indicator code (step 302). The time duration calculation is performed immediately after the progress indicator code is stored (step 304). The details of this calculation are given in FIG. 4. There is a particular progress indicator code that indicates the end of system initialization. If this "final" code is 5 detected (step 306) then the boot process is finished and the durations for each of the initialization tasks have been calculated and stored. If the progress indicator code is not the final code, then the next initialization task is performed (step 308) and control returns to step 302 where the progress indicator code is sent to the display buffer for the next task. [see column 4, lines 20-33]", "With reference now to FIG. 4, a flowchart shows the time 10 duration calculation in accordance with a preferred embodiment of the present invention. This figure is an expansion of step 304 shown in FIG. 3. The time duration is calculated for the initialization task that has been completed, hereafter called task one, and stores table entries for the task to be executed next, hereafter called task two. A complete description of the data stored in the table is given in FIG. 5 below. The progress indicator 15 code is read from the display buffer (step 402) and written to non-volatile random access memory (NVRAM). The current value of the processor time base register is read and written (step 404) to non-volatile random access memory (NVRAM). Hereafter, the value of the processor time base register is referred to as the time stamp. This value indicates the number of ticks of the processor clock. If nonvolatile RAM memory is not available yet, 20 then the progress indicator code and time stamp are stored in program RAM until, at a later time, NVRAM becomes available, and the information previously stored in program RAM is transferred to NVRAM at that time. Each task entered in the initialization table has three associated values: the progress indicator code, the time stamp when the task begins, and the calculated time duration in milliseconds. The duration calculation also 25 maintains a data entry point into the table so that data already recorded can be accessed and new data can be entered. The duration of task one is calculated when task two is ready to start (or when the initialization process is completed). The time stamp for task one is read from NVRAM (step 406) and used to calculate the elapsed time in milliseconds (step 408) for task one. [see column 4, lines 35-65]", "Column 502 contains the progress 30 indicator code for each task. Column 504 contains the time stamp value for each task,

which is the content of the processor time base register at the time the task was started. Column 506 is the calculated duration of each task in milliseconds. [see column 5, lines 8-13]". The initialization timing table (shown in FIG. 5) of Randall is utilized for self-test of each hardware during the boot time of a computer and calculating the elapsed

5 time of each task. The initialization timing table in FIG. 5 of Randall includes a plurality of rows, and each row is divided into three columns, which are columns 502, 504, and 506 respectively, where the three columns 502, 504, and 506 include progress indicator code, time stamp, and duration, respectively. Please also refer to FIG. 5 and to FIG. 6 of Randall as follows.

PROCESS INDICATOR CODE	TIME STAMP	DURATION
502	504	506
0100	000 050 000 000	2000
0202	000 450 000 000	900
0301	000 630 000 000	1100
0405	000 850 000 000	
:	:	:

500

INITIALIZATION TIMING TABLE  
*FIG. 5*

SAMPLE CALCULATION  
*FIG. 6*

PROCESSOR FREQUENCY : 200 MHz  
CONSTANT: 200,000 TICKS PER MILLISECOND  
TIME STAMP FOR TASK 0202 : 450,000,000  
TIME STAMP FOR TASK 0301: 630,000,000  
DURATION OF TASK 0202: 900 msec

$$\frac{630,000,000 - 450,000,000}{200,000} = \frac{180,000,000}{200,000} = 900 \text{ msec}$$

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In contrast, the initialization progress table of the present invention includes a plurality of fields for storing initialization states of each of a plurality of initialization regions of the RAID so as to indicate which initialization regions have been initialized by a regional initialization and which initialization regions have not yet been initialized. Thus, the initialization timing table of Randall is totally different from the initialization progress table of the present invention, although "the initialization timing table" of Randall is similar in name to "the initialization progress

table” of the present invention.

In addition, the applicant respectfully points out that the consistency initialization is also stated in claim 1 since claim 1 teaches “after the initialization progress table is 5 created and before the consistency initialization is completed, the RAID is allowed to be accessed while the consistency initialization is in progress”. Please refer to Fig 1. Fig. 1 shows an illustration of the consecutive initialization in the consistency initialization of the applicant’s invention, wherein the initialization initializes each region from 00000000H. The initialization progress table comprises four columns A, B, C, and D, 10 wherein the column A is an initialization region column (32-bits), the column B is a column indicating that the associated initialization region has been initialized (1-bit), the column C is a column indicating that the associated initialization region is being initialized (1-bit), and the column D is a column indicating that the associated initialization region has not been initialized yet (1-bit). The column A is utilized for 15 representing the regions in the memory, and the columns B, C, and D are utilized for representing the states of the regions. Each value 1 in the columns B, C, and D represents the corresponding region is in the corresponding state. For example, when a value in the column B is 1, it means the corresponding region has been initialized, when a value in the column C is 1, it means the corresponding region is being initialized, and when a value in 20 the column D is 1, it means the corresponding region has not been initialized yet. The columns B, C, and D can be a field stated in claim 1, and the field comprises 3-bits.

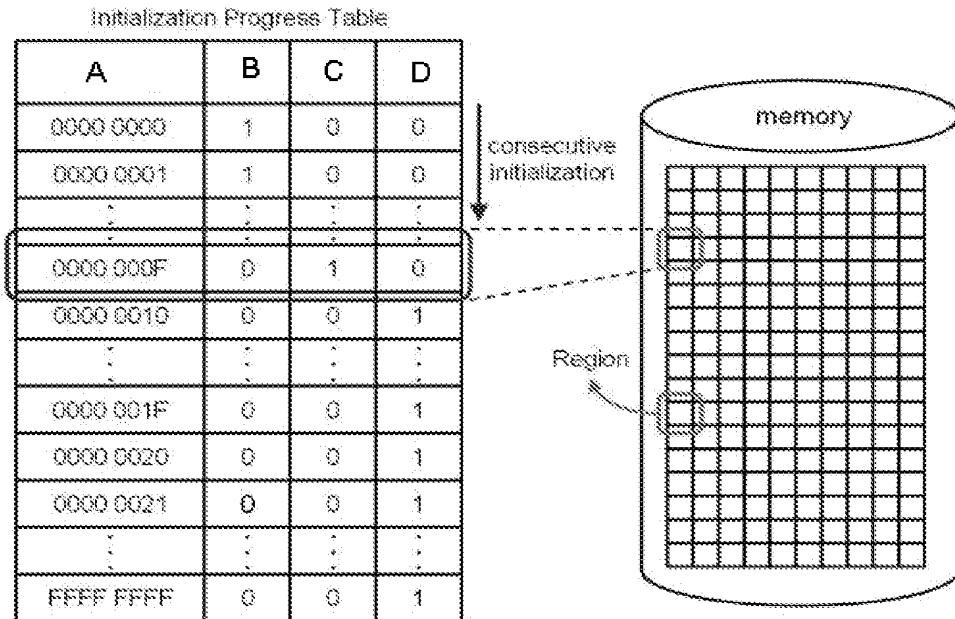


Fig. 1

Please refer to the following Fig. 2A and Fig. 2B. Fig. 2A and Fig. 2B show an illustration of the induced initialization of the applicant's invention. If an IO access is going to access a region, such as the region of 00000020H which has not been initialized yet, while performing the consecutive initialization, the induced initialization will be started. After the region of 000000FH has been initialized, it will next start to initialize the region of 00000020H.

Initialization Progress Table			
A	B	C	D
0000 0000	1	0	0
0000 0001	1	0	0
:	:	:	:
:	:	:	:
0000 000F	0	1	0
0000 0010	0	0	1
:	:	:	:
:	:	:	:
0000 001F	0	0	1
0000 0020	0	0	1
0000 0021	0	0	1
:	:	:	:
FFFF FFFF	0	0	1

Fig. 2A

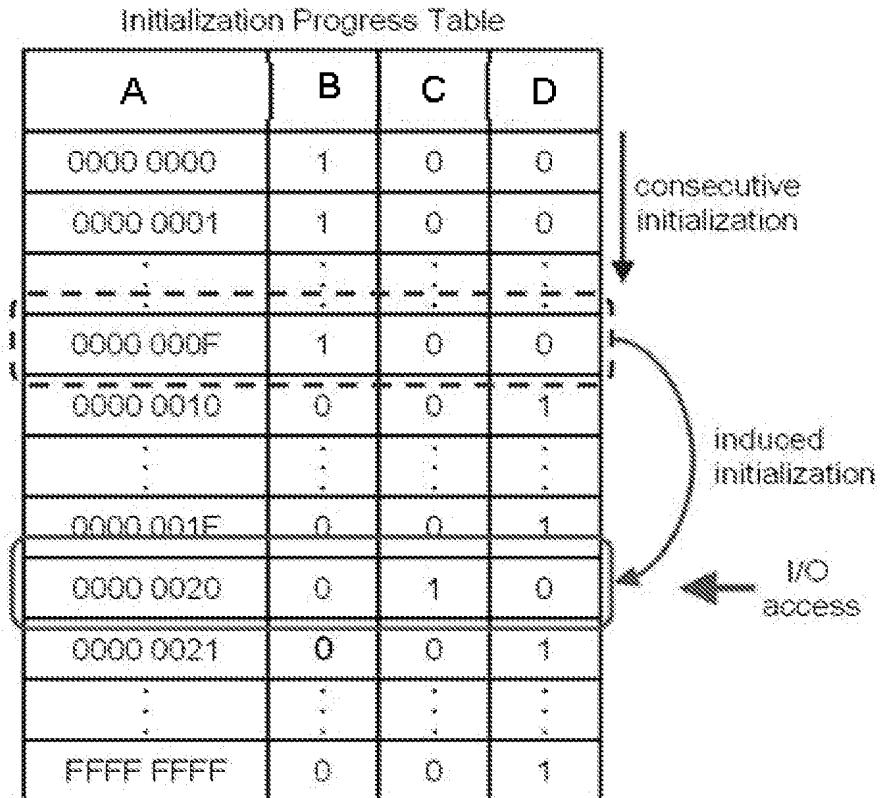


Fig. 2B

Thus, the applicant does not totally agree with Examiner's opinion directed to patentability of claim 1, and the applicant respectfully points out that the interpretations 5 of the initialization progress table and the consistency initialization have already been stated in claim 1. However, in order to speed up the prosecution of the instant application, claim 1 has been amended to specify that "data in the initialization regions of the RAID are made consistent with one another by the consistency initialization", so that the amended claim 1 is clearer and more patentably distinct from the cited references.

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In light of at least above reasons, the applicant asserts that claim 1 should be found allowable over the cited prior arts, and placed in condition for allowance. Withdrawal of the rejections under 35 U.S.C. 103(a) and consideration of the patentability of claim 1 is respectfully requested.

Claim 2-24

Claims 2-24 are dependent upon claim 1, and should be allowed if claim 1 is found allowable.

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**2. Conclusion**

Based on the above remarks, the applicant respectfully submits that all of the rejections set forth in the Office Action dated August 5, 2010 have been overcome and the pending claims are now in condition for allowance. The applicant therefore respectfully  
10 requests that a timely Notice of Allowance be issued in this case. If a telephone conference would facilitate the prosecution of this application, the Examiner is invited to contact the undersigned applicant's representative at the number indicated below.

Recognizing that Internet communications are not secure, I hereby authorize the USPTO to communicate with me concerning any subject matter of this application by  
15 electronic mail. I understand that a copy of these communications will be made of record in the application file.

Sincerely yours,

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/Scott Margo/

Date: 12/06/2010

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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 13 hours behind the Taiwan time, i.e. 9 AM in D.C. = 10 PM in Taiwan.)

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